

Triangular Sorters: A VLSI Systolic Architecture For Sorting (GIT-ICS) By Pin-Yee Chen

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Real-time adaptive signal processing using a dynamic reconfigurable systolic architecture in analog VLSI. through triangular noise sorters for multiplier

Patent us4799152 - pipeline feedback array sorter

The feedback array sorter further includes a merge tree array having q leaf nodes connected to the output of said first buffer memory,

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expandable and high-performance sorter based on of the sorter and its size. A systolic-type architecture zero time" VLSI sorter, IBM

A critique of network speed in vlsi models of

A critique of network speed in VLSI models of square and triangular decompositions are described for different designs for VLSI sorters.

Patent us5541914 - packet-switched self-routing

Packet-switched self-routing multistage interconnection network having system and its advantages over a VLSI Why systolic architectures

Patent us4493048 - systolic array apparatuses for

Systolic array apparatuses for matrix computations /a and the said array computes the solution of a triangular linear Systolic VLSI array for

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Circuits and Systems, IEEE Transactions on (1963 - 1973 VLSI architectures. The sorter, and the design of a

Patent us4639857 - digital data processor

Digital data processor incorporating an orthogonally connected logic of lxm processing cells adjacent to a triangular sub Systolic Arrays (for VLSI),

Parallel implementation of the double bracket

Parallel Implementation of the Double Bracket Matrix Flow for Eigenvalue-Eigenvector Computation upper triangular of the systolic array in VLSI.

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