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Patent us4639857 - digital data processor

Digital data processor incorporating an orthogonally connected logic of lxm processing cells adjacent to a triangular sub Systolic Arrays (for VLSI),

Presentation "spring 2006parallel processing,

Spring 2006Parallel Processing, Extreme ModelsSlide 2 About This Presentation
EditionReleasedRevised FirstSpring 2005Spring 2006 This presentation is intended to

Patent us4799152 - pipeline feedback array sorter

The feedback array sorter further includes a merge tree array having q leave nodes connected to the output of said first buffer memory,

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Presentation "winter 2014parallel processing,

Winter 2014Parallel Processing, Circuit-Level ParallelismSlide 1 Part II Circuit-Level Parallelism Part II Circuit-Level Parallelism 7.

Ieee xplore - conference table of contents

2014 IEEE International Symposium on; Circuits and In the analog VLSI implementation as well as the QRD-based triangular systolic array but

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HANDBOOK OF SENSORS AND ACTUATORS Series Editor: VLSI and Intelligent Transducers, shown in Figure 2, and 3-D systolic arrays, for example,

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On the design of a high-performance, expandable,

expandable and high-performance sorter based on of the sorter and its size. A systolic-type architecture zero time" VLSI sorter, IBM

Patent us4493048 - systolic array apparatuses for

Systolic array apparatuses for matrix computations /a and the said array computes the solution of a triangular linear Systolic VLSI array for

2010 ieee asia pacific conference on circuits and

VLSI implementation of a fast intra prediction algorithm for H.264/AVC encoding Systolic-array 3D wave-digital beam filters Panning sorter:

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Research Triangle Institute, "A bit-serial VLSI architectural An algorithm-based fault tolerance is achieved by testing the invariants of a systolic sorter

Slide 1

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Parallel implementation of the double bracket

Parallel Implementation of the Double Bracket Matrix Flow for Eigenvalue-Eigenvector Computation upper triangular of the systolic array in VLSI.

International journal of advanced research in

International Journal of Advanced Research in Proximity Coupled Equilateral Triangular Microstrip Design and Implementation of VLSI 8 Bit Systolic

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Reason - university of alberta

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Patent us5541914 - packet-switched self-routing

Packet-switched self-routing multistage interconnection network having system and its advantages over a VLSI Why systolic architectures

Dblp: ieee transactions on computers, volume 39

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Insertion Sorter Unit It sorts a Triangular systolic array with reduced latency for QR the 20th International Conference on VLSI Design jointly with the

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