

Triangular Sorters: A VLSI Systolic Architecture For Sorting (GIT-ICS) By Pin-Yee Chen

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Packet-switched self-routing multistage interconnection network having system and its advantages over a VLSI Why systolic architectures

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VLSI implementation of a fast intra prediction algorithm for H.264/AVC encoding Systolic-array 3D wave-digital beam filters Panning sorter:

Presentation "spring 2006parallel processing,

Spring 2006Parallel Processing, Extreme ModelsSlide 2 About This Presentation EditionReleasedRevised FirstSpring 2005Spring 2006 This presentation is intended to

Patent us4799152 - pipeline feedback array sorter

The feedback array sorter further includes a merge tree array having q leave nodes connected to the output of said first buffer memory,

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Proving (facts about) Ruby logic for describing and reasoning about systolic arrays. Taking triangular arrays as of a systolic sorter is formally

Slide 1

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Presentation "winter 2014parallel processing,

Winter 2014Parallel Processing, Circuit-Level ParallelismSlide 1 Part II Circuit-Level Parallelism Part II Circuit-Level Parallelism 7.

A critique of network speed in vlsi models of

A critique of network speed in VLSI models of square and triangular decompositions are described for different designs for VLSI sorters.

3g long term evolution baseband processing with

Insertion Sorter Unit It sorts a Triangular systolic array with reduced latency for QR the 20th International Conference on VLSI Design jointly with the

Parallel implementation of the double bracket

Parallel Implementation of the Double Bracket Matrix Flow for Eigenvalue-Eigenvector Computation upper triangular of the systolic array in VLSI.

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FOREWORD The VHSIC Program is currently in its seventh year, with only a few more challenging years to go. DoD and the Services have made tremendous strides in all of

Patent us4639857 - digital data processor

Digital data processor incorporating an orthogonally connected logic of lxm processing cells adjacent to a triangular sub Systolic Arrays (for VLSI),

Sceas

Real-time adaptive signal processing using a dynamic reconfigurable systolic architecture in analog VLSI. through triangular noise sorters for multiplier

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On the design of a high-performance, expandable,

expandable and high-performance sorter based on of the sorter and its size. A systolic-type architecture zero time" VLSI sorter, IBM

Parallel processing, part 2 - university of

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Systolic array apparatuses for matrix computations /a and the said array computes the solution of a triangular linear Systolic VLSI array for

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